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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,055	03/02/2004	Wei Guang Lu	X-1556 US	4741
24309	7590	10/05/2007		
XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124			EXAMINER COX, CASSANDRA F	
			ART UNIT 2816	PAPER NUMBER
			MAIL DATE 10/05/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/792,055

Applicant(s)

WEI GUANG LU

Examiner

Cassandra Cox

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-14 is/are allowed.
- 6) ☒ Claim(s) 1,2,7,15,16 and 21 is/are rejected.
- 7) ☒ Claim(s) 3-6,17-20 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 3/2/04.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7 and 21 are indefinite because it is not clear to the examiner how the coarse multiplexer module is coupled to output the zero phase shifted representation of the clock signal. Correction or clarification is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Kizer et al. (U.S. Patent No. 6,759,881).

In reference to claim 1 Kizer discloses in Figure 10 a digital high speed programmable delayed locked loop (DLL) comprises a zero degree phase shift digital delay line (415<sub>0</sub>, wherein the delay line is seen to have one delay element) operably coupled to produce, from a clock signal (202, 204), a zero phase shifted representation of the clock signal; at least one intermediate phase shift digital delay line (a first intermediate delay line being elements 415<sub>0</sub>-415<sub>1</sub>; a second intermediate delay line being elements 415<sub>0</sub>-415<sub>2</sub>; and a third intermediate delay line being elements 415<sub>0</sub>-415<sub>3</sub>) operably coupled to produce, from the clock signal, an intermediate phase shifted representation of the clock signal based on an intermediate control signal; a three hundred and sixty degree phase shift digital delay line (delay elements 415<sub>0</sub>-415<sub>4</sub>); and digital control module (403, 405, 407) operably coupled to produce the intermediate control signal and the three hundred and sixty degree control signal based on a phase difference between the zero phase shifted representation of the clock signal and the three hundred and sixty degree phase shifted representation of the clock signal.

In reference to claim 2 Kizer discloses in Figure 10 wherein the at least one intermediate phase shift digital delay line comprises: a plurality of intermediate phase shift digital delay lines (a first intermediate delay line being elements 415<sub>0</sub>-415<sub>1</sub>; a second intermediate delay line being elements 415<sub>0</sub>-415<sub>2</sub>; and a third intermediate delay line being elements 415<sub>0</sub>-415<sub>3</sub>).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizer et al. (U.S. Patent No. 6,759,881).

In reference to claim 15 Kizer discloses all the limitations of the claim as mentioned above with respect to claim 1, except Kizer does not disclose the programmable logic device comprising an input/output section including a digital clock management module; memory coupled to the input/output section; and programmable logic fabric coupled to the memory and the input/output section, wherein the digital clock management module includes a digital high speed programmable delayed locked loop. Programmable logic devices having an input/output section including a digital clock management module; memory coupled to the input/output section; and programmable logic fabric coupled to the memory and the input/output section, wherein the digital clock management module includes a digital high speed programmable delayed locked loop are well known in the art. It would have been obvious to one having skill in the art at the time of the invention that the delay locked loop of Kizer could be used in a digital clock management module of a programmable logic device for the advantage of providing multiple output clocks having controllable phase shifts.

In reference to claim 16 Kizer discloses in Figure 10 wherein the at least one intermediate phase shift digital delay line comprises: a plurality of intermediate phase shift digital delay lines (a first intermediate delay line being elements 415<sub>0</sub>-415<sub>1</sub>; a second intermediate delay line being elements 415<sub>0</sub>-415<sub>2</sub>; and a third intermediate delay line being elements 415<sub>0</sub>-415<sub>3</sub>).

***Allowable Subject Matter***

7. Claims 8-14 are allowed.

8. Claims 3-6 and 17-20 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Claims 3 and 17 would be allowable because the closest prior art of record fails to disclose a circuit wherein the plurality of intermediate phase shift digital delay lines comprises a ninety, one hundred and eighty, and two hundred and seventy degree phase shift digital delay line in combination with the rest of the limitations of the claims. Claims 4 and 18 would be allowable because the closest prior art of record fails to disclose a circuit wherein the input impedance of the zero phase shift digital delay line matches an input impedance of the at least one intermediate phase shift digital delay line and of the three hundred and sixty degree phase shift digital delay line in combination with the rest of the limitations of the claims. Claims 5-6 and 19-20 would be allowable because the closest prior art of record fails to disclose a circuit wherein the at least one intermediate phase shift digital delay line and the three hundred and sixty

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degree phase shift digital delay lines each comprise a coarse digital delay line, a coarse multiplexer, a fine digital delay line, and a fine multiplexer in combination with the rest of the limitations of the claims. Claim 22 would be allowable because the closest prior art of record fails to disclose a circuit wherein the circuit further comprises a plurality of multiplexers operably coupled to configure the delay lines in parallel for high speed operations and in series for lower speed operations in combination with the rest of the limitations of the claims.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*Cassandra Cox*  
Cassandra Cox  
September 30, 2007